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10 The SPARC Architecture Manual: Version 8. The current window is specified by the current window pointer (CWP) field in the processor state register (PSR). Window overflow and underflow are detected via the window invalid mask (WIM) register, which is controlled by supervisor software.

The SPARC Architecture Manual Version 8 - Cobham Gaisler

Note that the definition of this term is architecture-dependent and may differ from that used in other processor architectures. 2.14 f register: A floating-point register. SPARC-V9 includes single- double- and quad- precision f registers. 2.15 fccn: One of the floating-point condition code fields: fcc0, fcc1, fcc2, or fcc3.

The SPARC Architecture Manual - Department of Computer Science

The SPARC Architecture Manual Version 9 SPARC International, Inc. San Jose, California David L. Weaver / Tom Germond Editors SA-V09-R147-Jul2003 PTR Prentice Hall, Englewood Cliffs, New Jersey 07632.

The SPARC Architecture Manual - University of Wisconsin

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SPARC-V9 extends the addresses of SPARC to 64 bits and adds a number of new instructions and other enhancements to the architecture.1 SPARC-V9, like its predecessor SPARC-V8, is a microprocessor specification created by the SPARC Architecture Committee of SPARC International.

SPARC Architecture Manual Version9 - PDF Free Download

The SPARC Architecture Manual, Version 9 provides a complete description of the SPARC-V9 architecture. Since SPARC-V9 is an open architecture, many of the implementation decisions have been left to the manufacturers of SPARC-compliant processors. These "implementation dependencies" are introduced inThe SPARC

UltraSPARC User's Manual (UltraSPARC-I, UltraSPARC-II)

xii SPARC Assembly Language Reference Manual November 1995. This document describes the language in which the source files must be written. The nature of the machine mnemonics governs the way in which the program's executable portion is written. This document includes descriptions of the pseudo operations that allow control over the object file.

SPARC Assembly Language Reference Manual - cse.scu.edu

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SPARC Assembly Language Reference Manual Sun Microsystems, Inc. 4150 Network Circle Santa Clara, CA 95054 U.S.A. Part No: 816-1681-10 ... program modules intended to exploit features of the SPARC architecture in ways that cannot be easily done using high level languages and their compilers.

SPARC Assembly Language Reference Manual

The SPARC Architecture Manual, Version 8 For implementors of the SPARC 32-bit architecture and developers of SPARC system software (i.e. simulators, compilers, debuggers, and operating systems), including developers writing in assembly language.

Technical Documents | SPARC International, Inc.

to the Oracle SPARC Architecture 2015 Draft D1.0, 30 Jun 2016 Privilege Levels: Privileged and Nonprivileged Distribution: Public Part No. Release 1.0, 2002 ... SPARC M7 supports up to a eight way glueless (without external hub chips) coherent system using 7 coherence link channels. SPARC M7 has 32 SPARC physical processor cores.

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